ABSTRACT

A computer system with a plurality of peripheral busses is adapted to permit multicast signals to be transmitted by a device on one peripheral device to multiple devices on the other peripheral bus in a single bus cycle. In an exemplary embodiment, two PCI busses are provided, and master devices on either bus are capable of transmitting multicast signals to multiple targets on either bus. Targets of a multicast cycle are identified by a target identification signal on a first and a second multicast bus. A bus bridge relays the data for the multicast cycle between bridges. In an exemplary embodiment, a sideband signal from the master to the bridge indicates a multicast signal has been transmitted on the bus. In response, the bridge relays the multicast data to the other bus, while also transmitting a sideband signal to devices on the second bus indicating multicast data is being transmitted on that bus. Targets identified on that bus than capture the multicast data.